

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. BP 1907)

In re Application of: John Lin et al.

Serial No. 10/008,872

Filed: November 8, 2001

For: Master to Multi-Slave
Asynchronous Transmit FIFO

Group No./AU: 2188

Examiner: Duc T. Doan

EXAMINER'S AMENDMENT

IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1 1. (Currently Amended) A wireless transceiver device, comprising:
 - 2 modulation circuitry for modulating and demodulating signals that are transmitted over airwaves;
 - 3 frequency conversion circuitry for up converting and down converting between radio frequency
 - 4 signals and baseband frequency signals;
 - 5 digital-to-analog conversion circuitry for converting from analog to digital and from digital to
 - 6 analog;
 - 7 a radio controller;
 - 8 baseband processing circuitry including a first in, first out (FIFO) memory structure for storing
 - 9 addresses for accessing data blocks; and
 - 10 a plurality of command blocks formed within a memory structure, the command blocks include
 - 11 addresses of data blocks stored within random access memory and a memory portion for storing an
 - 12 indicator for storing an indicator indicating whether a command block of the plurality of command blocks
 - 13 is in use.

Claim 2. (Cancelled)

- 1 3. (Previously Presented) The wireless transceiver device of claim 1 wherein the FIFO memory
- 2 structure includes pointers that define addresses of the command blocks.

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Claim 4. (Cancelled)

- 1 5. (Previously Presented) The wireless transceiver device of claim 1 wherein the modulation
- 2 circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry.

- 1 6. (Previously Presented) The wireless transceiver device of claim 1 wherein the frequency
- 2 conversion circuitry converts directly between radio frequency and baseband.

- 1 7. (Previously Presented) A method for storing and transmitting data, comprising:
 - 2 storing a data block in random access memory; and
 - 3 storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure,
 - 4 the pointer includes an address of a command block;
 - 5 storing an address of the data block in the command block; and
 - 6 setting an indicator signal in a defined memory location, wherein the indicator signal indicates
 - 7 that the data block address stored in the command block is for data that has yet to be successfully
 - 8 transmitted and that the command block is busy.

Claims 8-10. (Cancelled)

- 1 11. (Previously Presented) The method of claim 7 wherein an address for a data block is only stored
- 2 in a command block if the indicator signal reflects that the command block does not contain the address
- 3 of a data block that has yet to be successfully transmitted.

- 1 12. (Currently Amended) The method of claim 7 further comprises:
 - 2 evaluating the address of the command block address included within the FIFO pointer.

- 1 13. (Previously Presented) The method of claim 12 further comprises:
 - 2 examining the contents of the command block specified by the pointer to determine a data block
 - 3 address.

- 1 14. (Previously Presented) The method of claim 13 further comprises:
 - 2 evaluating at least a first memory location of the data block whose address is stored in the
 - 3 command block to determine a data block size.

- 1 15. (Previously Presented) The method of claim 14 further comprises:
 - 2 retrieving an amount of data corresponding to the data block size and transmitting that data to a
 - 3 radio modem for transmission over wireless airwaves.

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1 16. (Previously Presented) The method of claim 15 further comprises:
2 resetting the indicator signal if the transmission was successful.

1 17. (Currently Amended) A memory structure formed within a baseband processing system,
2 comprising:

3 a random access memory portion for storing data blocks that are to be transmitted in a first in,
4 first out (FIFO) order; and a FIFO memory structure for storing pointers that correspond to the data
5 blocks stored in the random access memory portion;

6 a plurality of command blocks defined within the random access memory portion wherein each
7 command block is for specifying an address of a data block that is to be transmitted; and

8 a defined memory portion ~~for storing command block indicators~~ storing command block
9 indicators for each command block, wherein the command block indicators specify whether its
10 corresponding command block includes the address of a data block that has yet to be transmitted
11 successfully.

Claims 18-19. (Cancelled)

1 20. (Currently Amended) The memory structure of claim 17 wherein the defined memory portions
2 ~~for storing the command block indicators~~ storing the command block indicators are each one bit in length.

1 21. (Previously Presented) The memory structure of claim 17 wherein the command blocks defined
2 within the random access memory portions are each four bytes in length.

1 22. (Currently Amended) The memory structure of claim 17 wherein the FIFO memory structure
2 defines a plurality of FIFO memory ~~blocks wherein each blocks, wherein each~~ blocks, wherein each FIFO memory block
3 relates to data blocks that are to be transmitted to a particular device.